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Batch Fabrication of High-Performance Planar Patch-Clamp Devices in Quartz

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We report here on a batch microfabrication approach for producing ultra-smooth, high-aspect ratio structures in silicon dioxide and quartz films, and we apply that method towards the construction of planar-patch clamp electrophysiology devices that, for the first time, achieve the performance metrics of the very best micropipette-based patch-clamp approaches.

The patch-clamp method has been a powerful technique for elucidating ion channel protein biophysics and for assisting drug discovery, since its invention by Neher and Sakmann.[1] This technique traditionally involves bringing a flame-polished glass micropipette into contact with a cell membrane and electrically isolating a membrane patch (**Figure 1a**). The high resistance of the seal (>1 GΩ is the gold standard) minimizes leakage conductance and thus Johnson noise, allowing one to probe single ion channels and macroscopic (whole-cell) ion channel activity with high signal to noise. The modification of channel activity using chemical and physical stimuli, has, for example, yielded a deeper understanding of how membrane proteins link internal cellular activity with the extra-cellular environment.[2] However, the technique is serial and time consuming, prompting investigators to develop wafer-based approaches to patch-clamping to increase the throughput of measurements (Figure 1b).[3,4]

The success of the glass micropipette patch-clamp technique has implicated glass or quartz as the favored material for microelectrodes.[5] Typical micropipettes have tip openings 0.5–2.0 μm wide. Additionally, the cell membrane is drawn 5–100 μm into the pipette,[6] suggesting that there is a lower limit to the depth of a planar pore that can be utilized as a patch-clamp electrode. High density plasma etching is preferred for micromachining SiO_2 films due to its enhanced etch-rate, uniformity, anisotropy, and selectivity over masking and underlying layers.[7] However, high biases are required when plasma etching high aspect ratio (HAR) structures in dielectrics,[8] and this makes the realization of smooth HAR pores in glass difficult (Figure S1; Supporting Information). This hurdle has driven several groups to build planar patch-clamp platforms in alternative materials, such as silicon[9–13] and polydimethylsiloxane (PDMS).[14–17] Alternatively, groups have also explored non-standard, serial microfabrication techniques such as ion track etching,[18] ion milling,[19] and laser machining[20] through SiO_2 films. Some of these platforms have yielded GΩ seals in over 50% of trials, with typical seal resistances in the range of 1–5 GΩ, and rarely exceeding 10 GΩ.[11,16,18,20] These values are lower than what is possible with the micropipette approach. For high resolution, single-ion channel measurements (Figure 1c), seals in excess of 20 GΩ are desired.[1,21] Furthermore, many planar devices exhibit relatively high open electrode resistances of 6–30 MΩ,[11,16,17] which can introduce a large $R_{series}C_{mem}$ noise that can interfere with whole cell measurements (see Figure 1c).[22] Devices fabricated in a quartz-like material (which has a lower dielectric loss factor than silicon, PDMS, and other glasses[23]) with a low open electrode resistance, and that routinely achieve seal resistances >10 GΩ would be preferred for high resolution measurements of single (1–2 pA) and whole cell ion channel currents.

We report here on a combined electrochemical/lithographic process that defines highly polished micrometer and submicrometer-sized features in thick metal masking films. These films are utilized as etch masks during the high density plasma etching of silicon dioxide (also an electrochemical process). We show, through experiment and theory, that the thickness of the conducting masking film modulates, in a unique way, the electric field within the HAR dielectric. This, in turn, permits the degree of ion bombardment to the mask/oxide sidewall to be tailored, and allows for the realization of smooth HAR pores in fused quartz and deposited low temperature oxide (LTO). Smooth HAR pores 7–12 μm deep in fused quartz/silica with open electrode resistances in the range of 0.8–3.0 MΩ are demonstrated, and GΩ seals are achieved in nearly 80% of trials, with the majority exhibiting seal resistances from 20–80 GΩ. The resultant planar patch-clamp array is competitive with the best of pipette-based patch-clamp measurements. Furthermore,

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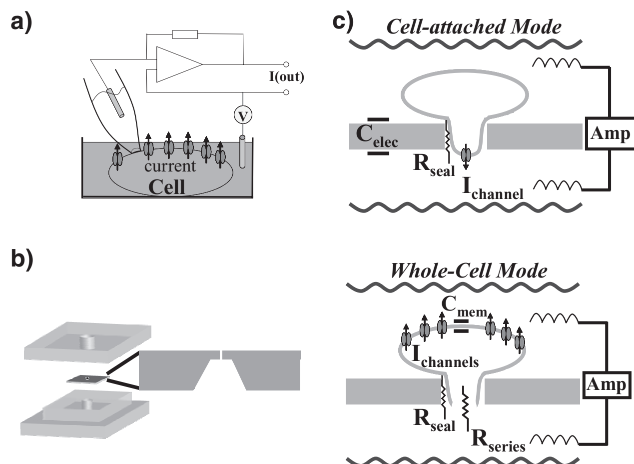

Figure 1. Patch-clamp platforms. a) The traditional patch-clamp technique allows the 'clamping' of membrane voltage and recording of ion channel current from single cells by 'sealing' a 1–2 μm diameter, flame-polished, glass pipette to the cellular membrane and utilizing electronic feedback circuitry. b) A planar patch-clamp electrode replaces the glass pipette with a wafer-based device with a small pore through the wafer. The pipette solution is below the wafer while the extracellular solution is above the wafer. c) In cell-attached mode, a high resistance seal ($R_{seal} > 1$ GΩ) minimizes leakage conductance and thus Johnson noise, allowing one to probe single ion channel activity. In this recording configuration the noise is dominated by the seal resistance and by the capacitance of the patch-clamp electrode. In whole-cell mode the patch is ruptured, allowing voltage clamping of the entire cell membrane, and thus the measurement of macroscopic ion channel activity. In this recording configuration, with $R_{seal} > 1$ GΩ, the noise is dominated by the $R_{series}C_{mem}$ combination.

the microfabrication procedures are consistent with established integrated circuit parallel fabrication approaches.

We begin by depositing Ni films of various thicknesses onto a SiO_2 substrate, onto which a 230–270 nm thick resist film is deposited via spin-coating. An array of holes is first defined within the resist, using electron beam or UV lithography. These holes are smaller diameter than the desired final pore size, a design consideration that compensates for undercut during the subsequent electrochemical process (**Figure 2a**).[24] To electrochemically etch the Ni, the substrate (anode) is immersed in 85% H_3PO_4(aq) and a positive bias is externally applied to the exposed metal. The relatively low water concentration (14.2 M) of the H_3PO_4(aq) is exploited to limit the etch rate and to polish the metal sidewalls: the rate-limiting step is the diffusion of water to the metal surface to dissolve reaction products.[25,26] As a consequence, raised features on the metal surface are etched faster because they are exposed to a higher local water concentration. This suppresses any influence that crystallographic orientation and/or surface defects could have on the anodic dissolution rates.[24] Care must be taken so that the edges of the exposed Ni do not etch faster than the center of the pattern – a condition that can result in island formation. Conditions that discourage island formation are a thicker resist layer and/or metal film, a smaller diameter resist pattern, and lower applied bias.[27] The proper choice of conditions permits the reproducible production of ultrasmooth pores, with sub-micrometer and micrometer-sized diameters, in Ni films ranging from 100–600 nm thick (Figure 2b). (See Experimental Section and Supporting Information for details).

Inductively-coupled plasma reactive ion etching (ICP-RIE) is employed to transfer the Ni patterns into the underlying SiO_2 layer (Figure 2c). C_4F_8(g) is the main feed gas for SiO_2 etching due to its appreciable etch rate and selectivity.[28] The ICP etching system utilizes a coil to decouple the plasma density from the ion energy, which is independently-controlled.[7] While increased ICP powers generally result in improved etch rates, reproducibility will suffer, especially at the micrometer and sub-micrometer scale. A relatively low ICP power of 1000 W was utilized to minimize thermal fluctuations of the etching chamber wall and hence, fluctuations in fluorocarbon deposition onto the wafer during the etching process.[29] This, in turn, resulted in highly reproducible etching conditions (Figure S2; Supporting Information).

ICP-RIE etching of the substrates, when masked with the smooth Ni pores, enables us to realize HAR SiO_2 pores with very smooth sidewalls (Figure 2d). When we varied the Ni mask thickness for a particular SiO_2 etching time, we observed an unexpected trend: the oxide pore sidewall smoothness increased as the Ni mask thickness increased (**Figure 3a**). Even with an RIE P of 500 W with a 500 nm thick Ni mask, the silicon dioxide sidewall remained very smooth (Figure S3; Supporting Information). These results are counter-intuitive since thicker metal masks with their more tapered sidewalls are more prone to mask erosion, and hence, micro-masking which can produce rougher oxide sidewalls during plasma etching.[30] The electric charging of HAR oxide structures masked with insulating films during high density plasma etching has been previously shown to affect etching.[31,32] However, the effects of metal masks have largely been ignored. Thus, we sought to better understand the plasma etching of HAR structures that were masked with conducting films.

Monte Carlo simulations were utilized to investigate the plasma etching trends described above. We considered only electrical charging effects. This assumption is likely valid because we are etching in the SiO_2 sputtering regime (etch bias ~378–434 V),[28] and we found that a variety of experimental plasma chemistries produced the same result: the sidewall smoothness increased with the thickness of the conductive mask (Figure 3a and Figure S3, Supporting Information). Because it was impossible to know the exact experimental plasma conditions (e.g., ion energy distribution, ion and electron temperature, plasma density), we investigated trends. We simulated charging within a dielectric pore geometry for different aspect ratios (by altering the mask thickness; Figure S4; Supporting Information). Insulating and conducting mask cases were investigated and compared.

Consider first the typical case of utilizing a high-density plasma to etch a HAR dielectric structure, with an insulating thin film as the etch mask. The flux of electrons that penetrate deep into the HAR structure will decrease with increasing depth due to the isotropic velocity distribution of the electrons (Figure S5a; Supporting Information), and thus, negatively charge the top portions of the mask sidewall. In addition to this geometric shadowing, the negative charges on the sidewall will repel additional electrons, serving to further reduce the flux of electrons to the pore bottom, at least initially. The trajectory of the positive ions however, is not significantly perturbed by the negative

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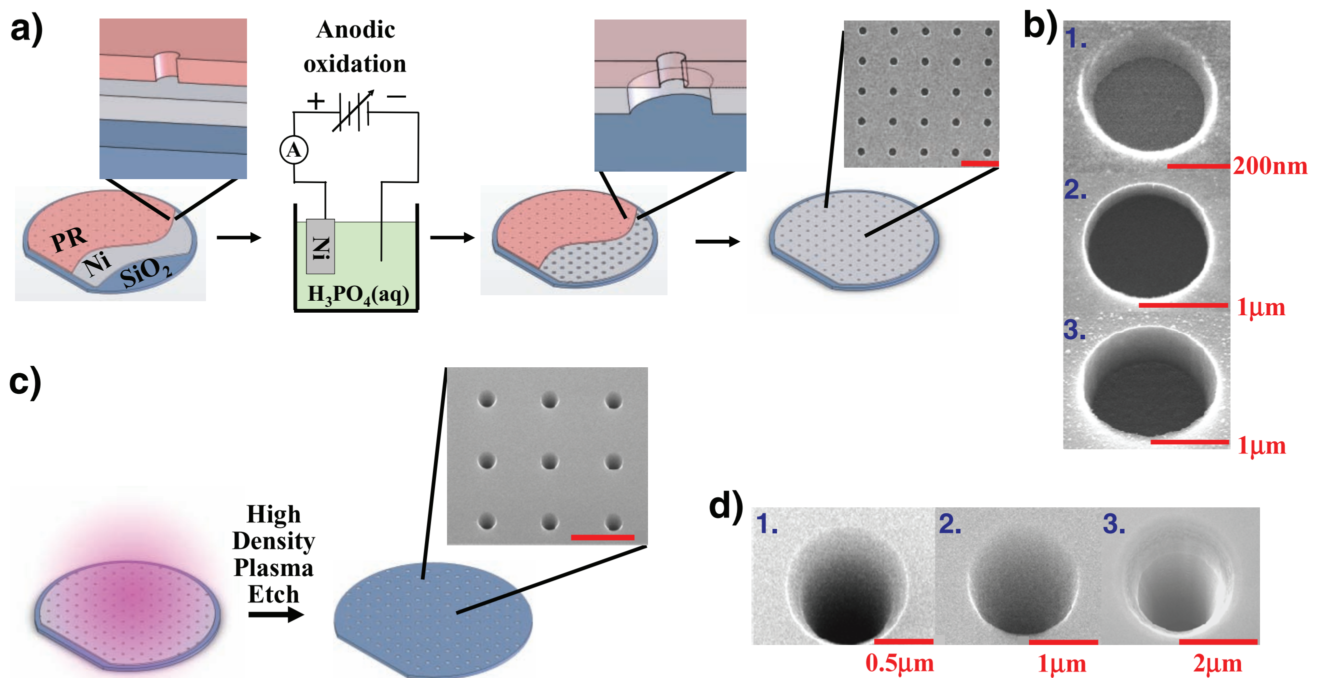

Figure 2. Highly polished, lithographically-defined structures in metal and dielectric films. a) Pore patterns, smaller than the intended nickel pores, are lithographically defined in a resist layer above a nickel film. The exposed Ni (anode) is electrochemically etched/polished in concentrated acid to create highly polished Ni patterns undercut from the resist pattern. SEM image of arrays of pores in a 250 nm thick Ni film is shown. Scale bar = 5 μm. b) SEM images of pores in Ni films with different thicknesses, #1-3: 100 nm, 300 nm, 500 nm, respectively. c) The Ni pores serve as etch masks during high-density plasma etching of high aspect ratio structures in silicon dioxide. An SEM image of an array of pores etched 5μm deep in silicon dioxide. Scale bar = 5 μm. d) SEM images of high-aspect ratio pores in silicon dioxide with very smooth sidewalls. The depth of each pore, #1-3, is 3 μm, 5 μm, 8 μm, respectively. Pores #1-2 are etched in LTO films while pore #3 is etched in fused quartz.

sidewall due to the ions' greater translational energies. Thus, the ions, owing to their anisotropic velocity distribution, positively charge the bottom surface of the pore. Consequently, the potential within the trench rises as a function of depth to attract electrons and repel positively charged ions in order to balance the reduced electron current (Figure S6a; Supporting Information). This continuous rising potential in the pore results in retarding, local electric fields throughout the pore at steady state ($\overline{E} = -\overline{\nabla}\phi$) (Figure 3b).[31,33–36]

When the aspect ratio of the pore is increased to 1.5 (by increasing the insulating mask thickness), the current imbalance becomes more severe. As a result, the positive potential at the bottom of the pore will increase to greater values, deflecting more ions towards the upper insulating sidewalls to cancel negative charges. This allows relatively more electrons to be attracted deeper into the pore at steady state. Because the mask and pore sidewall are both insulating, the electron flux (Figure S5a; Supporting Information) and potential (Figure S6a; Supporting Information) change in a gradual and uniform manner throughout the pore depth and across the pore width (i.e. there are no significant potential gradients towards the sidewalls).[36] This is evident by observing the similarity and uniformity of the local electric fields throughout the pore for two different aspect ratios (Figure 3b).

Now consider the situation in which a metallic etch mask is used. Unlike with an insulating mask, electrons are lost when they collide with the conductive mask ($\phi_{surface} = 0$). As the thickness of the metallic mask is increased, a large fraction of the electrons will collide with the mask sidewall since there are no negative charges to repel electrons. The same fundamental response as with the previous case arises; if the balance of ion and electron currents to the insulating surface is perturbed, the surface responds by charging up so that a new current balance is established.[36] In this case, the upper sidewalls of the dielectric region charge to very significant positive values to increase the potential in the center of the mask/dielectric pore interface region, allowing more electrons to flow into the dielectric pore while deflecting ions into the mask at steady state (Figure S5b and S6b; Supporting Information). The large potential gradients result in the formation of substantial, retarding electric fields in the mask/dielectric interface region (Figure 3c).

To appreciate the degree that these large electric fields protect the oxide sidewall from excessive ion bombardment during plasma etching, incident ion energies were calculated for both the insulating and conducting mask case at a pore aspect ratio of 1.5 (thicker mask). The ion incident energies for a conducting mask at the top of the pore are significantly lower relative to an insulating mask (Figure 3b and 3c). The potential change through the pore at the centerline, however, is similar for both cases (Figure S6c; Supporting Information). Consequently, the conducting mask enables plasma etching of ultrasmooth, dielectric HAR structures with an appreciable etch rate.

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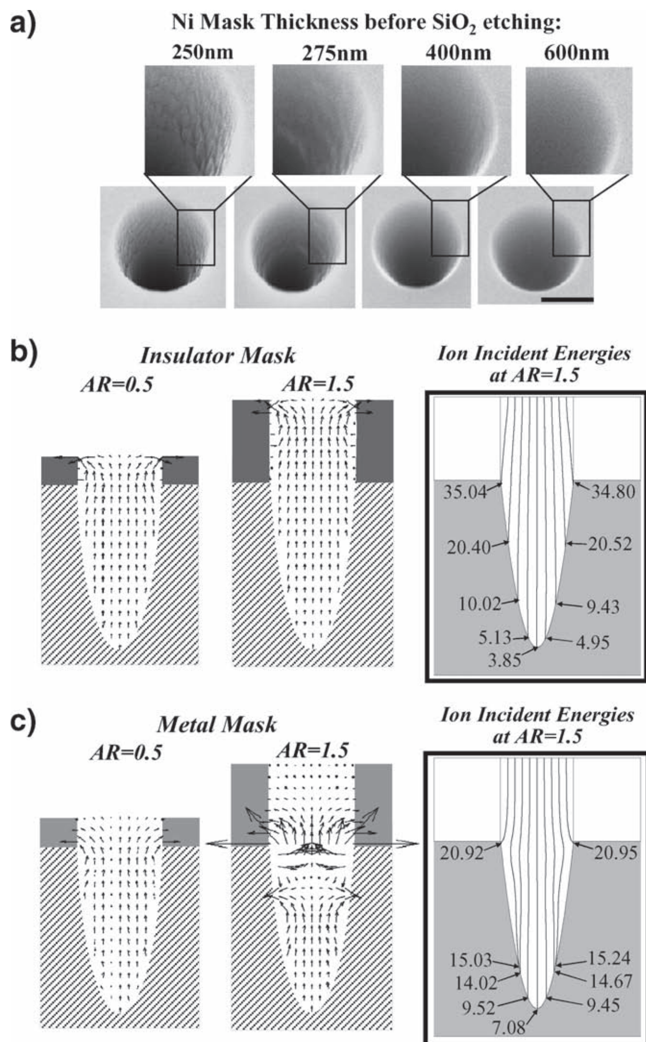

Figure 3. Monte Carlo simulations of electric charging in HAR structures during plasma etching. a) SEM images of pores etched in silicon dioxide with identical etching parameters masked with four different Ni film thicknesses, showing a trend of increased silicon dioxide sidewall smoothness with increased Ni mask thicknesses. Scale bar = 1 µm. b) Monte Carlo simulations of the electric fields that develop within high aspect ratio dielectric structures during plasma etching with different insulating mask thicknesses. c) Electric field plots for metal masks. Incident ion energies in electron volts (eV) were calculated for both insulating (b) and conducting (c) masks, from an initial ion energy of 65 eV.

We utilized HAR pores suspended in silicon dioxide membranes as planar patch-clamp electrodes (Figure 1b). The following pore geometries (depth × diameter, in micrometers) were tested: 0.5 × 1.5, 1.5–2.6 × 1.2–1.6, 3.0 × 0.6–1.0, 5.0 × 0.7–2.9, and 7.6–12 × 1.1-5.1. The 0.5 µm and 1.5-5.0 µm deep pores were fabricated in thermal oxide and LTO films on silicon, respectively, while the 7.6–12 µm deep pores were fabricated in fused quartz. With the experimental setup shown in Figure 1b, cells were introduced into the top chamber and suction from the bottom chamber was applied until a cell was immobilized and sealed over the pore. Seal resistances (Figure 1c) were recorded by applying a voltage pulse and monitoring the leakage current.

The yield of GΩ seals did not depend upon pore diameter over the range studied (although the open electrode resistance is related to the diameter), but rather to pore depth (**Figure 4a**). GΩ seals were only obtained for pore depths ≥5 µm (Figure 4b), demonstrating that there is a glass surface area threshold to obtain GΩ seals. This likely means that the seal resistance is distributed along the cell membrane/glass surface interface.[6,37] With pores >7 µm deep, GΩ seals were achieved in nearly 80% yield, with the majority of seals over 20 GΩ and as high as 80 GΩ. Most GΩ seals with pores >7 µm deep were stable for at least 30 minutes, with several lasting longer than 60 minutes. Because planar patch-clamp pores fabricated in borosilicate (a low loss dielectric) with an outward taper have been reported to rarely achieve seals in excess of 5 GΩ,[18] and borosilicate micropipettes with a very small diameter and more narrow taper have been reported to achieve seals >50 GΩ,[21] we hypothesize that the enhanced performance of our planar devices is due to the slightly inward taper of the etched pore (Figure 2d) which may favor a more intimate contact between the glass surface and cell membrane.

We present recordings of ion channel current in whole cell mode (Figure 1c) from a voltage-clamped RBL-1 cell with a 5 µm deep planar pore (Figure 4c). Our wafer packaging scheme (Figure 1b) is currently designed for quick exchange of patch-clamp electrode chips in order to test the yield of GΩ seals; consequently, it draws too much capacitance for high resolution single ion channel measurements. The seal resistance was 10 GΩ before transitioning into whole cell mode. The current-time traces (Figure 4c) and current-voltage relation (Figure 4d) are characteristic of inward rectifying potassium (IRK) channels. The zero current at 0 mV indicates that the predominant ion channel conductance is carried by K^+ ions since $[K]_{internal} = [K]_{external}$, in agreement with the literature.[38]

A combined lithographic and electrochemical method was developed to pattern highly polished micrometer sized features through thick Ni films. This process should be further applicable to other metals[39,40] and metal alloys.[24] Polished features in Ni films were used as etch masks for the plasma etching of HAR structures into silicon dioxide. We demonstrate that the thickness of the conducting mask modulates the electric field within the HAR dielectric during plasma etching, and allows for the tailoring of the sidewall smoothness, which ultimately enables the realization of smooth, HAR pores in glass and fused quartz. In addition to electrophysiology, the microfabrication approaches developed here may have applications in other fields, such as photonics[41] and plasmonics.[42,43]

HAR pores in quartz, when utilized as planar patch-clamp electrodes, exhibit unrivaled wafer-based patch-clamp performance. A high yield of GΩ seals is achieved, with most of those seals exhibiting a resistance in excess of 20 GΩ, and as high as 80 GΩ. When interfaced with a microfluidic system, these devices should enable the acquisition of high quality single ion channel data.[16,44] Furthermore, the high performance of these devices does not come at a cost of large open electrode resistances. Finally, microfabrication steps utilized here are amenable to batch fabrication, and thus have the potential to serve as the foundation for an ultra-low noise, high throughput patch-clamp platform.

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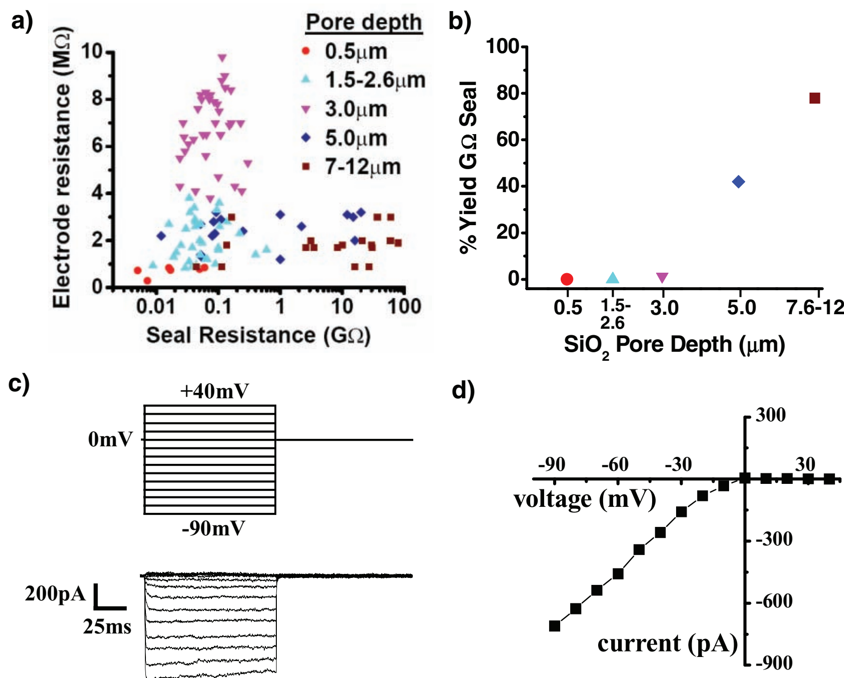

Figure 4. High performance planar patch-clamp electrodes. a) A plot of open electrode resistance versus maximum seal resistance is shown for various values of pore depth. b) Plot showing relation between % yield of GΩ seals and pore depth. c) Whole cell current of inward rectifying ion channels endogenously expressed in RBL-1 cells is recorded with a 5 µm deep planar patch-clamp pore. The voltage protocol is shown above. d) Current vs. voltage plot of the whole cell ion channel current from c).

Experimental Section

Ni film anodic etching: Ni was evaporated onto polished wafer substrates at a rate of 1 Å s^{-1} with a Mark 40 Electron-Beam Evaporator (CHA Industries, Fremont, CA). Either electron-beam or photolithography was used to pattern features into the resist film. The Ni surface was contacted with an 'alligator' clip on the top of the wafer, while the rest of the wafer was submerged into Class 10 85% (wt) phosphoric acid (General Chemical; Parsippany, New Jersey). Biases were applied to the substrates with an E3611A DC Power Supply (Agilent Technologies; Inc, Santa Clara, CA). See Table S1 in the Supporting Information for exact processing parameters.

High-density plasma etching of SiO_2: Patterns in the nickel masking film were transferred into the SiO_2 with an Advanced Oxide Etcher (Surface Technology Systems, PLC; Newport, UK) after a chamber cleaning and seasoning. Unless noted, the plasma parameters were ICP $P = 1000$ W, $C_4F_8 = 40$ sccm, $O_2 = 5$ sccm, $p = 6$ mT. See Table S2 in the Supporting Information for exact processing parameters.

Monte Carlo simulations of HAR dielectric etching: Monte Carlo simulations of charging during plasma etching have been previously described.[31] A specific dielectric pore geometry is assumed (Figure S4a; Supporting Information) while the mask thickness is varied, thus, altering the aspect ratio.

Cell culture and harvesting: All cell lines and reagents were purchased from the American Type Culture Collection (ATCC; Manassas, VA). Cells were grown and passaged according to the ATCC guidelines. Before electrophysiology measurements, cells were spun down at 500–800 RPM and washed with saline three times.

Electrophysiology recordings with planar electrodes: The wafer packaging scheme, electrophysiology setup, and cell-loading/seal-testing procedure has been previously described.[9] When testing seals, the intracellular solution (bottom-side) contained (in mM) 130 KCl, 5 NaCl, 2.5 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, pH = 7.4 with a final osmolarity of 265 mOs. The extracellular solution contained (in mM) 130 NaCl, 5 KCl, 10 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, pH = 7.4 (adjusted with NaOH) with a final osmolarity of 293 mOs. For the whole cell measurement in Figure 4c, the intracellular solution contained (in mM) 130 KCl, 5 NaCl, 4 $CaCl_2$, 2.1 $MgCl_2$, 10 HEPES, 10 EGTA with $pH = 7.4$. The extracellular solution contained (in mM) 130 KCl, 5 NaCl, 10 $CaCl_2$, 2 $MgCl_2$, 10 HEPES, $pH = 7.4$. The current traces in Figure 4c were acquired at 20 kHz and filtered at 1 kHz.

Supporting Information

The Supporting Information contains a detailed protocol of the fabrication, simulations, and electrophysiology methods. The Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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